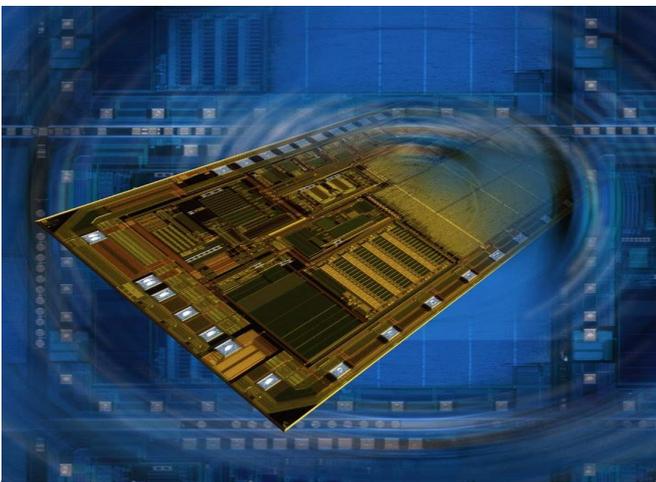


Product Information Interface for Ignition Drivers – CK110

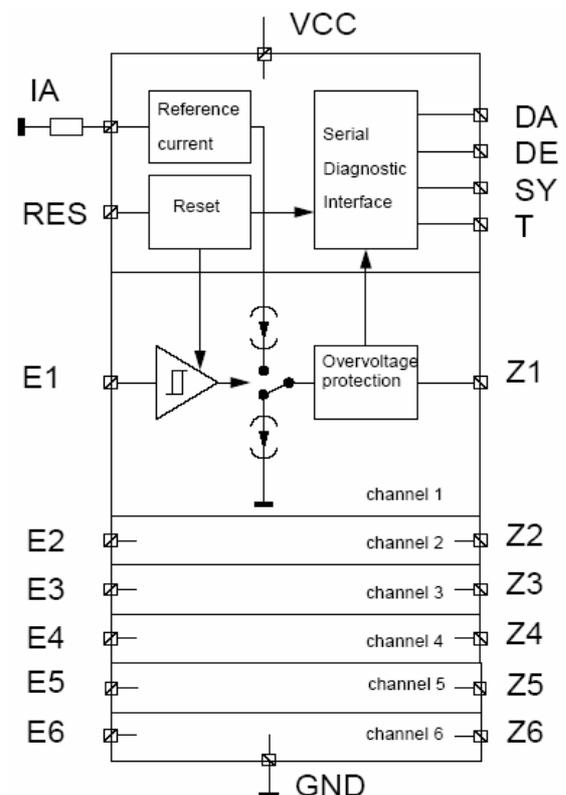


Interface for Ignition Drivers

Customer benefits:

- ▶ Excellent system know-how
- ▶ Smart concepts for system safety
- ▶ Secured supply
- ▶ Long- term availability of manufacturing processes and products
- ▶ QS9000 and ISO/TS16949 certified

Block- / functional diagram



The CK 110B / UC10B is an inverting driver for ignition stages.

Features

- ▶ 6 identical current sources , the level is adjustable by an external resistor, with input level LOW the sources on Z1-Z6 are active
- ▶ 6 identical Low side switches with input level HIGH these switches Z1-Z6 are active
- ▶ Generating an internal reference current, which depends on an external resistor, and which adjusts the level of the current sources
- ▶ Reset input RES , with LOW on RES , the low side switches at Z1-Z6 are active
- ▶ Undervoltage detection the low side switches at Z1-Z6 are active
- ▶ Serial diagnostic interface

Maximum ratings

Parameter	Min	Max	Unit
Junction temperature T _J	-40	150	°C
Storage temperature T _C	-55	125	°C
Maximal ambient temperature: T _{Umax} = T _{Jmax} - (P _V * R _{THJC}) with R _{THJC} = 85K/W P _V = V _{CC} * I _{VCC} + (V _{CC} -U _{Z1}) * I _{source} + U _{Z1} * I _{sink} + ... + (V _{CC} -U _{Z6}) * I _{source} + U _{Z6} * I _{sink} (Per channel only I _{source} or I _{sink} is active)			
Power supply static V _{CC} for maximal one hour in lifetime	0 5.5	5.5 6.5	V V
Maximal voltage at the driver outputs U _{ZAi} (without influence to other channels or to diagnosis)			
static	- 2	18	V
dynamic (t < 10ms)	-5	18	V
Limit for TRISTATE V _{CC}		>3	V

Functional description

Driver for ignition stages

The CK110B / UC10B is an interface between processor and ignition stages.

6 driver outputs can be controlled by 6 inputs.

With input level LOW a current source is activated, with input level HIGH a low side switch is activated.

It's possible to activate more than 1 driver at the same time.

Within the maximum ratings the circuit includes a short circuit protection to UBAT and to ground.

At the outputs a maximum capacitance of 10nF is allowed (47nF R = 30Ω).

The current level of all sources is adjustable by an external resistor at pin IA to ground.

The dependency is:

$$I_{source} = (V_{CC} * 100V) / (R_{IA} * 5V) \quad 4.5k\Omega < R_{IA} < 30k\Omega$$

The maximum current level of the low side switch is fixed (typ. 45mA).

Because of the power consumption this current will be reduced at short circuit to UBAT (typ. 2.8mA).

With the input RES the low side switches of all driver outputs are activated.

Ei	Res	Outputs Zi
X	0	low side switch active
0	1	source active
1	1	low side switch active

X : can be 0 or 1

The inputs E1-E6 and RES include internal pull up current sources.

An undervoltage detection activates all low side switches if the power supply voltage is less than typ. 3,8V (hysteresis typ. 50mV).

At a power supply voltage less than max. 3V the outputs can have a high impedance state.

Serial diagnostic interface

The CK110B / UC10B includes a diagnostic circuit for each channel which detects short circuit to ground (KSM) short circuit to UBAT (KSUB) and open load(LA). The detection works only when the current source is activated. When the low side switch is activated no diagnosis is possible.

If an error occurs the first time an internal counter is started. The error states of the different channels are stored after the delay time in an internal shift register and can be read out with the serial interface.

If there is a change of error condition the internal shift register will be updated directly without a delay time.

An error state in the shift register is indicated with a LOW on the interface output DA (only when SY is HIGH).

If a failure has been stored in the shift register and the failure condition disappears the last detected failure remains stored.

If the SY-signal is LOW the different diagnostic bits can be read out with an external clock at pin T.

Each channel has 2 bits in the shift register where the 3 possible error states can be indicated.

For the 6 channels 12 bits are needed. To have an easier software for the processor the number of bits in the shift register is 16. The fixed level of the 4 unneeded bits is HIGH.

After the transmission the shift register will be reset with the change of the SY signal from LOW to HIGH. A new error entry is possible after the delay time when the error condition occurs.

It's possible to cascade the diagnostic interface. Also in this case the DA output changes to LOW when there is an error entry in any shift register (SY is HIGH).

The output DA of the diagnostic interface is an open drain output.

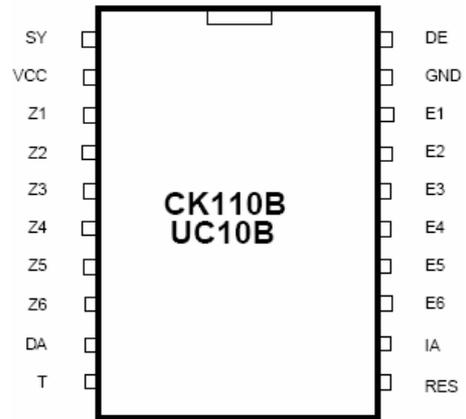
The input DE has a pull up current source.

Logic table of the diagnostic interface

R	SY	DE	T	DA	Shift register
L	H	H	X	H	reset, no diagnosis possible
L	H	L	X	L	reset, no diagnosis possible
L	L	X	X	H	reset, no diagnosis possible
H	H	L	X	L	error entry possible
H	H	H	X	H/L	error entry possible
H	L	X	L	H/L	1.Bit on DA , with clock on T it's possible to read the shift register, no error entry possible

PIN configuration

Package: SOIC20L



Pin description SOIC20L

Pin	Description
E1 to E6	Inputs to switch the driver
Z1 to Z6	Driver outputs
RES	Reset active with LOW
IA	External resistor to adjust the current source level
DA , DE , T , SY	Pins for serial diagnostic interface
VCC	Power supply 5V
GND	Ground

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