Coside Testcase: ATOM SOMP

AE/PAI-IP | 2023-11-10

BOSCH

Coside Testcase: ATOM SOMP

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Coside Testcase: ATOM SOMP
Agenda

- ATOM introduction
  - ATOM Channel Architecture
  - ATOM Channel Configuration
- Coside testcase introduction
  - Installation
  - Structure
  - Execution
- Coside testcases clarification
  - Code
  - Waveforms

** This document is based on the GTM specification and is available on our website: https://www.bosch-semiconductors.com/ip-modules/gtm-platform/gtm-generic-timer-ip-module/*

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01

ATOM introduction

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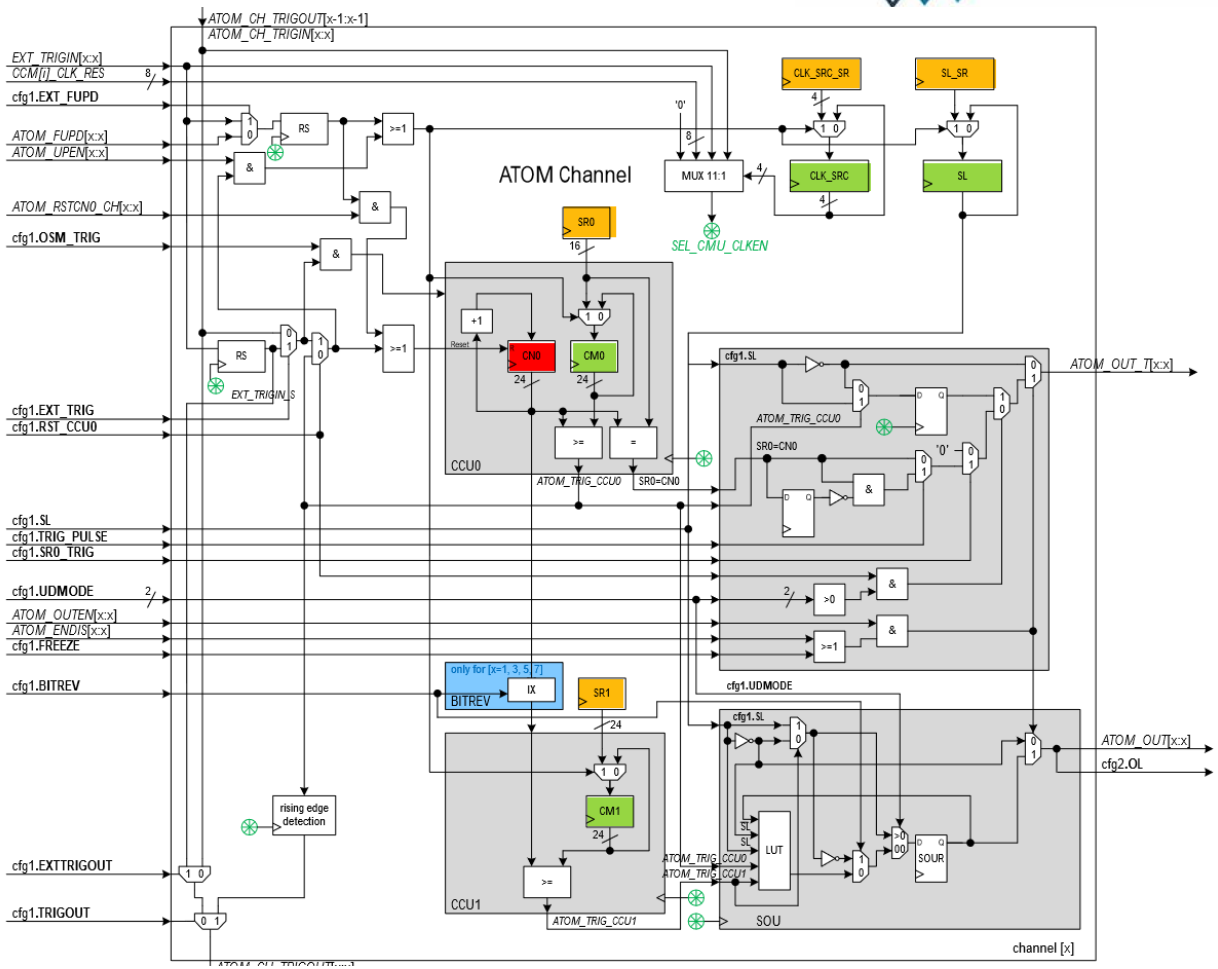
Coside Testcase: ATOM SOMP
ATOM Channel Architecture

- Counter register
  - CN0
- Operation registers
  - CLK_SRC, CM0, CM1
  - SL
- Shadow registers
  - CLK_SRC_SR, SR0, SR1
  - SL_SR (only available for GTM4)
- Frequency from CCM_CLK_RESx



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Coside Testcase: ATOM SOMP
ATOM Channel Configuration – SOMP mode

- In **S**ignal **O**utput **M**ode **P**WM (SOMP) mode, the ATOM channel can generate complex PWM signals with different pulse widths and periods by configuring different operation registers, and possibly update the parameters synchronously with the shadow registers.
  - CM0
    - Sets the period value of PWM and can be updated with the content of the shadow register SR0
  - CM1
    - Sets the pulse width value of PWM and can be updated with the content of the shadow register SR1
  - CN0
    - Counts until it reaches CM0-1 and it is then reset to 0 in continuous counting up mode
  - CLK_SRC
    - Determines the clock resolution of the counter can be updated with the content of the shadow register CLK_SRC_SR
  - SL
    - Decides ATOM output signal level
    - Can be updated with the content of the shadow register SL_SR (only available for GTM4)

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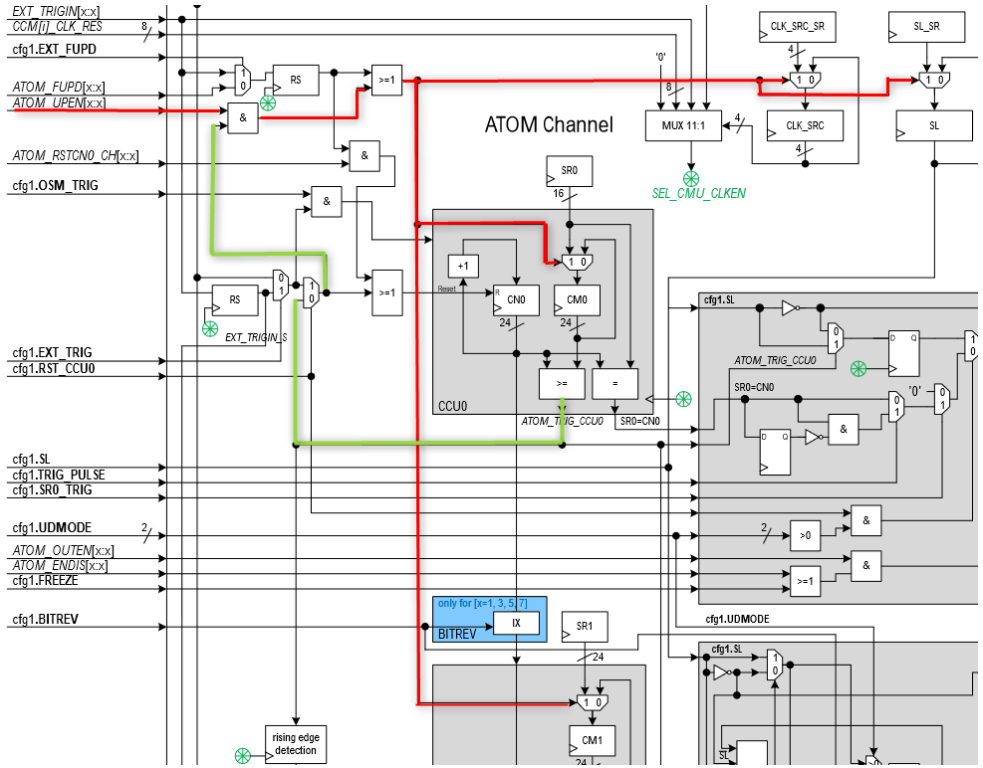
Coside Testcase: ATOM SOMP
ATOM Channel Configuration – Update Mechanisms

- Available options of update mechanisms for pulse width (SR1→ CM1) period (SR0 → CM0) and clock frequency (CLK_SRC_SR → CLK_SRC)
  - UPEN
  - FUPD
  - EXT_TRIGIN

- UPEN signal to update data in the provided testcase
  - UPEN enable signal
  - UPEN trigger signal
    - ATOM_TRIG_CCU0=1 when the compare match



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02

Coside testcase introduction

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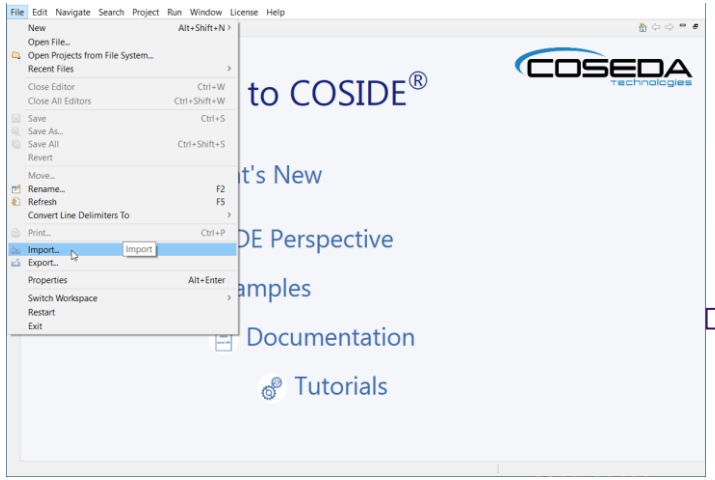
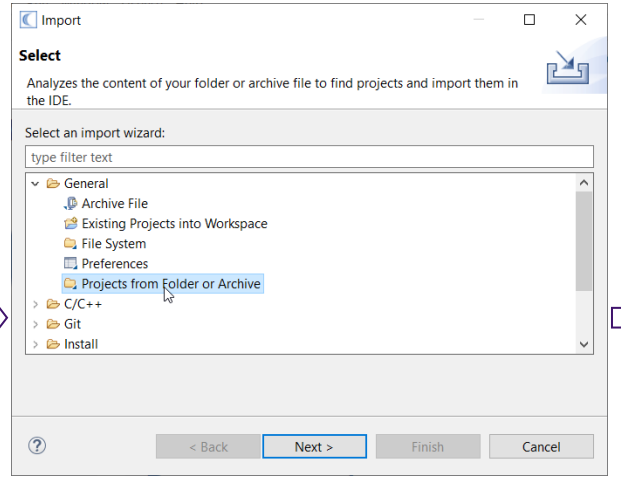
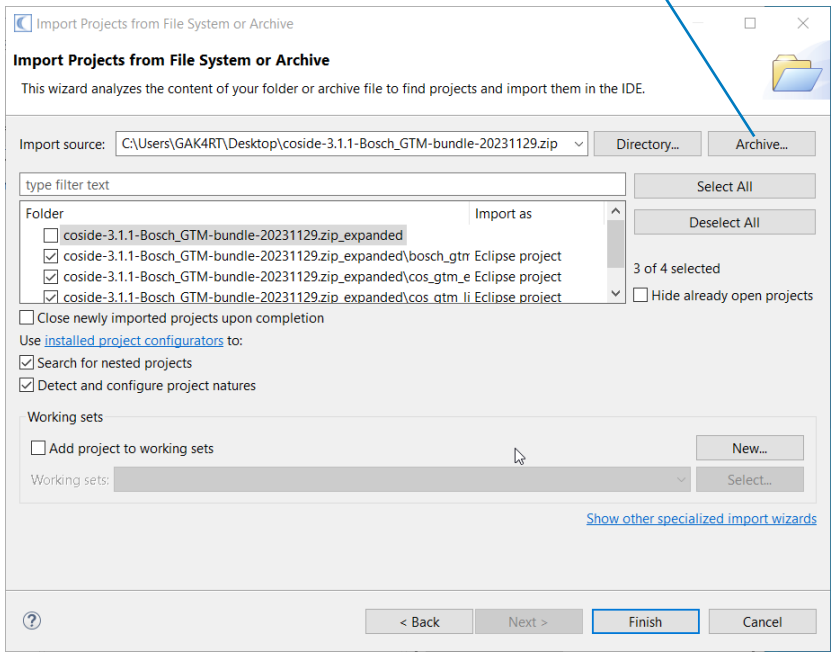
Coside introduction
Installation

- Import the virtualGTM in a new Coside workspace





Select VirtualGTM.zip file in the correct archive



Close the help center page

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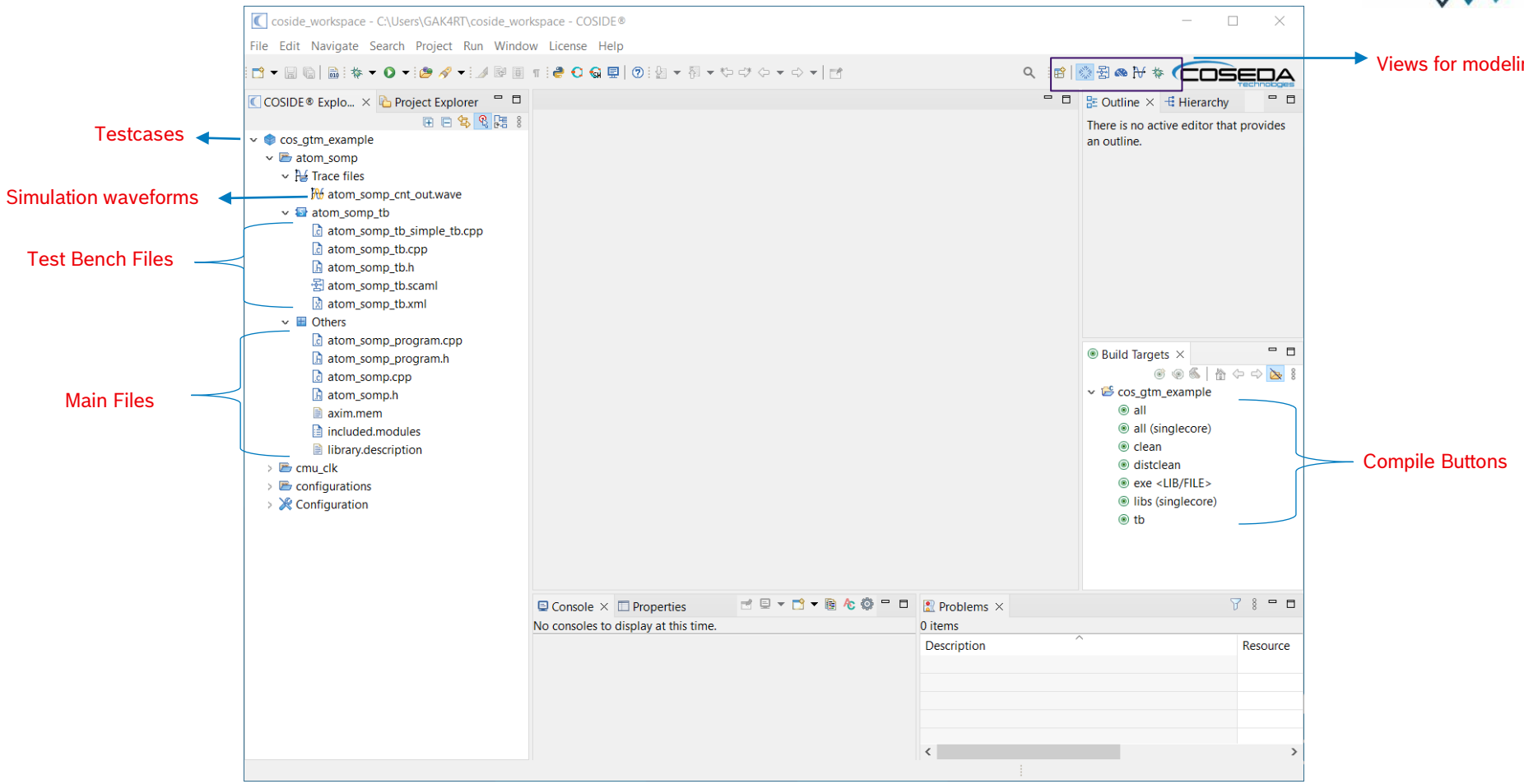
Coside Testcase: ATOM SOMP
Structure



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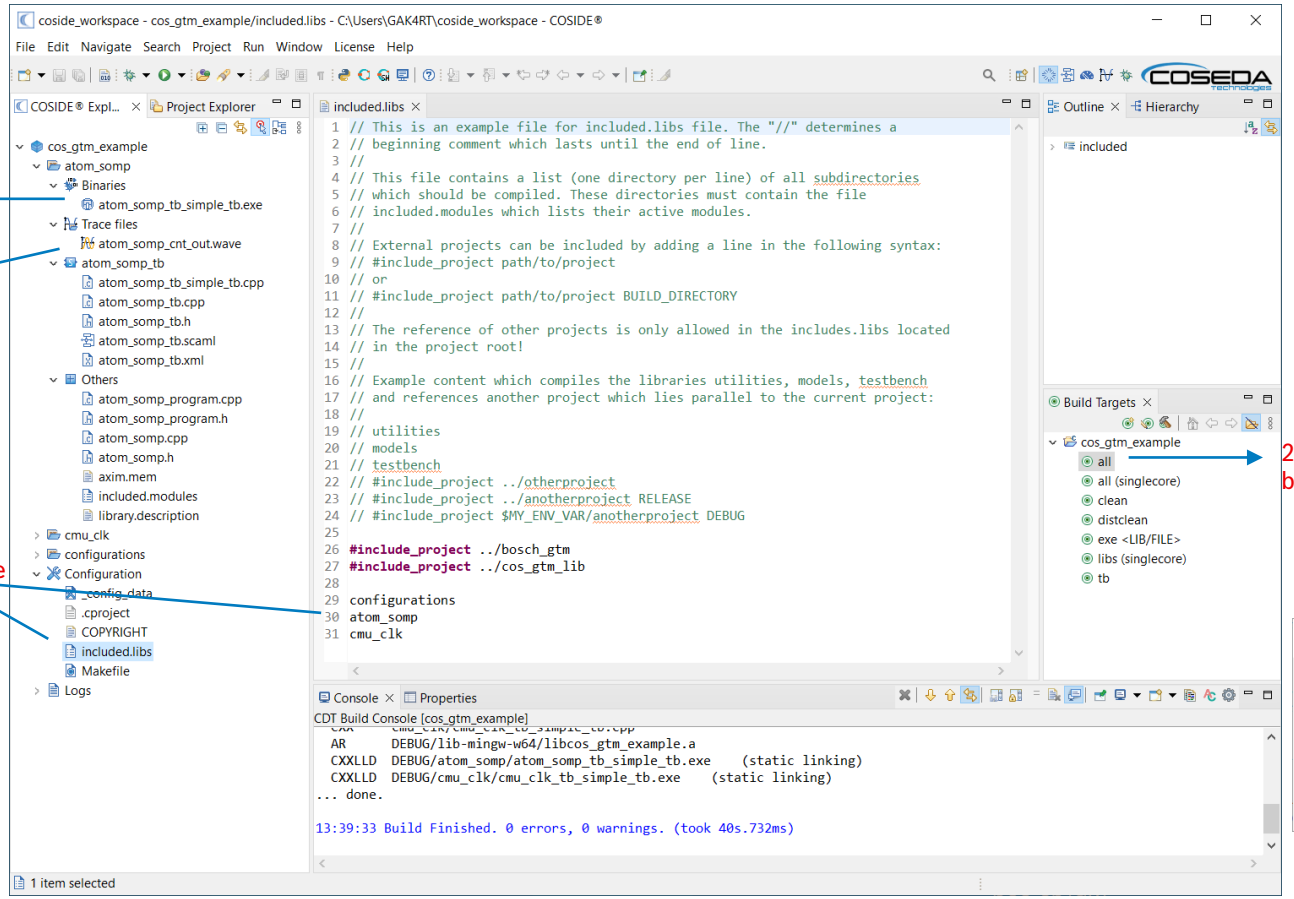
Coside Testcase: ATOM SOMP
Execution

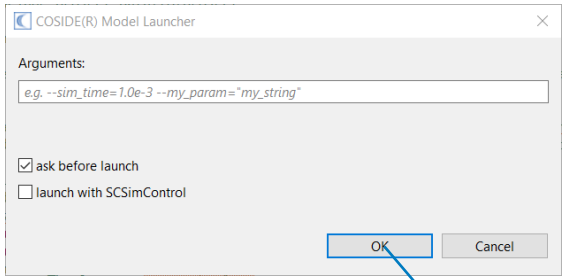


3. Double-click the **.exe file** to execute the test case

5. Open **.wave files** to see the simulation waveforms

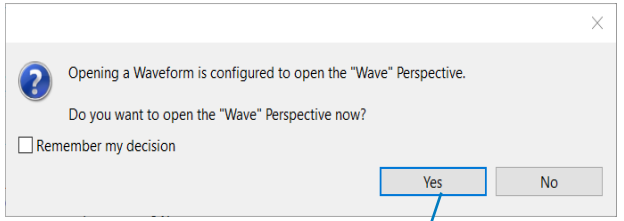
1. Write and save testcase name in **included.libs**

(Skip this step if the name already in it)



4. Click **OK** button

2. Double-click **all** button to build cos_gtm_user



6. Click **Yes** button

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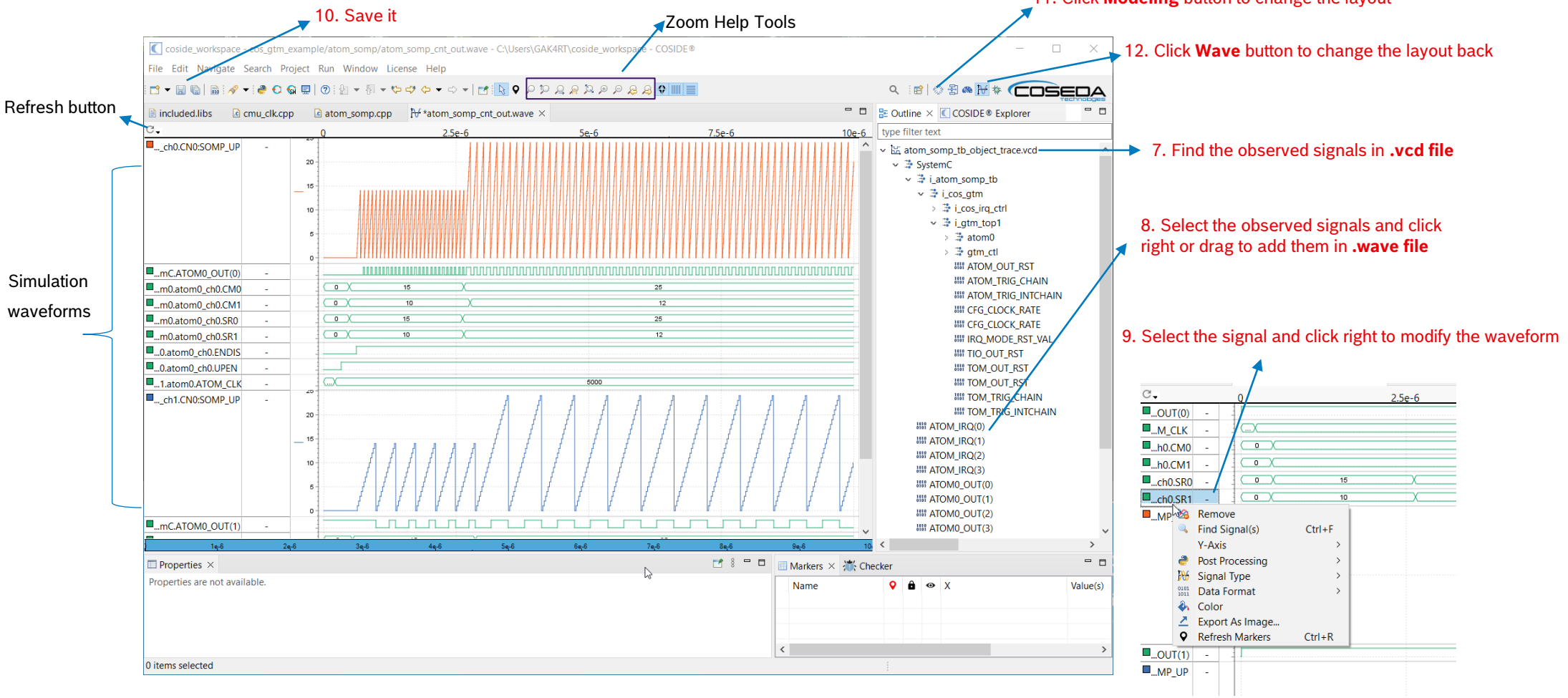
Coside Testcase: ATOM SOMP
Execution



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03

Coside testcases clarification

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Coside Testcase: ATOM SOMP

Code – atom_somp.cpp

LAB definition

To execute LAB1, modify the code to #define LAB 0x1 and then recompile it

Cluster clock configuration

Cls_clk is divided by 1 and works at full (GTM) clk (200 MHz)

Module clock configuration

CMU_CLK_RES[0:0] is divided by 1 and works at 200 MHz

CMU_CLK_RES[1:1] is divided by 5 and works at 40 MHz

Enabling UPEN

Values in shadow registers can be updated in the operation registers

ATOM Channels configuration

CH0 uses the CMU_CLK_RES[0:0], CH1 uses the CMU_CLK_RES[1:1]

Both channels work in the SOMP mode

```
21 #define GAL_COMPATIBILITY_H_
22 #include <gal_app.h>
23
24 #define LAB 0x0
25
26 #ifdef COSIDE
27 namespace atom_somp
28 {
29 #endif
30
31
32 int atom_somp()
33 {
34     GAL_INFO("COS_GTM_USER local definition");
35  GAL_INFO("Configure cluster clocks ... switch off cluster 1..n");
36  int cls_div= 1;
37  GTM.CLS[0].ARCH.CTRL = 0x0;
38  GTM.CLS[0].ARCH.CLK_CFG = cls_div & 0x03 ;
39
40
41     GAL_INFO("GTM_REV = 0x%08X", (uint32_t) GTM.CLS[0].ARCH.REV );
42
43     GAL_INFO("configure CMU");
44     GAL_INFO("============================================================");
45     // Set Count Value for clock devider
46     GTM.CLS[0].CMU.CLK_0_CTRL = 0;
47     GTM.CLS[0].CMU.CLK_1_CTRL = 4;
48
49     // Enable CMU_CLK0 and CMU_CLK1
50     GTM.CLS[0].CMU.CLK_EN = 0x0000000A;
51
52
53     GAL_INFO("configure ATOM channel 0 and 1");
54     GAL_INFO("============================================================");
55
56     // Enable update of compare register (SR -> CM)
57     GTM.CLS[0].ATOM.AGC.GLB_CTRL= 0x000A0000;
58
59
60 #if GAL_GTM_GEN > 3
61     GTM.CLS[0].ATOM.CH[0].CTRL_SR = 0x00000000; // clk_src = CMU_CLK_0
62 #endif
63     GTM.CLS[0].ATOM.CH[0].CTRL = 0x00000002;    // clk_src = CMU_CLK_0,  SOMP (Bit 1:0 = 0b10)
64 #if GAL_GTM_GEN > 3
65     GTM.CLS[0].ATOM.CH[1].CTRL_SR = 0x00001000; // clk_src = CMU_CLK_1
66 #endif
67     GTM.CLS[0].ATOM.CH[1].CTRL = 0x00001002;    // clk_src = CMU_CLK_1,  SOMP (Bit 1:0 = 0b10)
```


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Coside Testcase: ATOM SOMP

Code – atom_somp.cpp

```
69      // Set Shadow and Compare Register
70  #if LAB == 0x1
71      GTM.CLS[0].ATOM.CH[0].CM0 = 150;                // initial delay
72      GTM.CLS[0].ATOM.CH[0].CM1 = 100;                //
73  #endif
74      GTM.CLS[0].ATOM.CH[0].SR1 = 10;             // SR1 = duty cycle
75      GTM.CLS[0].ATOM.CH[0].SR0 = 15;             // SR0 = period
76      GTM.CLS[0].ATOM.CH[1].SR1 = 10;
77      GTM.CLS[0].ATOM.CH[1].SR0 = 15;
78
79      GAL_INFO("start signal generation on ATOM channel 0 and 1 running in SOMP mode");
80      GAL_INFO("============================================================");
81      // Enable ATOM Output and Channel 0 and 1
82      GTM.CLS[0].ATOM.AGC.OUTEN_STAT = 0x0000000A;
83      GTM.CLS[0].ATOM.AGC.ENDIS_CTRL = 0x0000000A;
84
85      // Set Host Trigger to update ENDIS_STAT
86      GTM.CLS[0].ATOM.AGC.GLB_CTRL = 0x00000001;
87
88      gal_wait(2);
89      GAL_INFO("--> change PWM period and duty cycle");
90      GTM.CLS[0].ATOM.CH[0].SR0 = 25;
91      GTM.CLS[0].ATOM.CH[0].SR1 = 12;
92      GTM.CLS[0].ATOM.CH[1].SR0 = 25;
93      GTM.CLS[0].ATOM.CH[1].SR1 = 12;
94
95      gal_wait(4);
96      return 0;
97  }
98
99  //---------------------------------------------------------------------------
00  //---------------------------------------------------------------------------
01
02
03  void atom_somp_isr()
04  {
05      GAL_INFO("Interrupt service routine");
06  }
07
08
09  #ifdef COSIDE
10  }
11  #endif
12
```

PWM initial delay set

LAN0: Without setting the initial delay ; LAB1: initial delay is 150 clock cycles

PWM parameters written in shadow registes

ATOM channels enable

Global enable and output enable

Trigger request

Updated ENDIS_STAT to make the ATOM Channels are enabled atomic

New PWM parameters written in shadow registers

Placeholder for interrupt routines

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Coside Testcase: ATOM SOMP
Waveforms – LAB0

- Tasks
  - Generates a PWM signal with 10 clock cycles pulse width and 15 clock cycles period
  - Updates PWM characteristics with 12 clock cycles pulse width and 25 clock cycles period
  - PWM period and pulse width values are updated by the UPEN signal
  - Uses different clock resolutions for CH0 and CH1, but same PWM parameters -> different PWM

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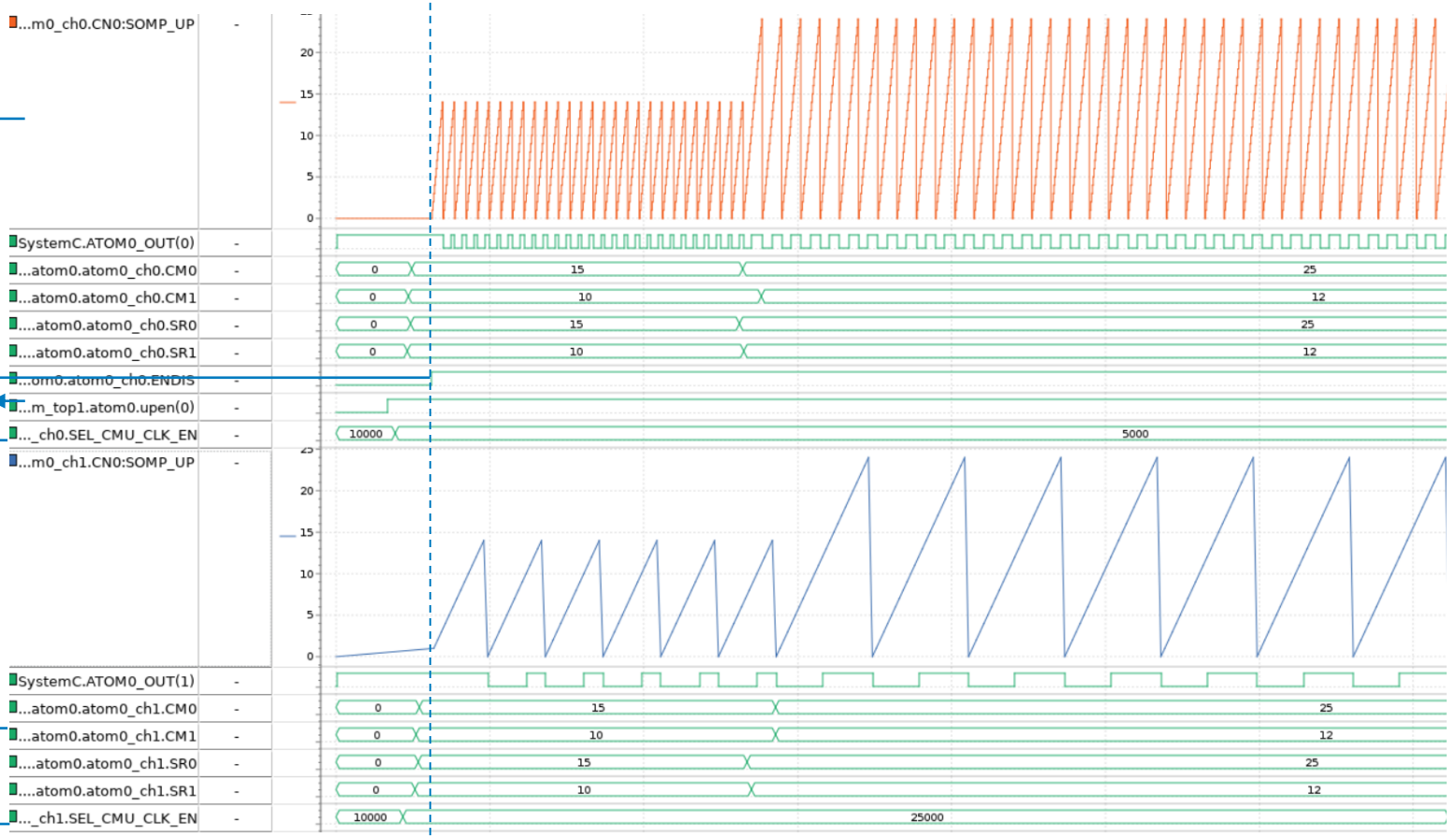
Coside Testcase: ATOM SOMP
Waveforms – LAB0



Continuous counting up mode counter

After enabling channels, the counter starts counting

After enabling UPEN, SR0->CM0, SR1->CM1

CH0 works at 5 ns

CM0-> PWM period

CM1-> PWM pulse width

CH1 works at 25 ns

ATOM_CH0

ATOM_CH1

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Coside Testcase: ATOM SOMP
Waveforms – LAB1

- Tasks
  - Based on the LAB0 (without changing any parameter) initial delay is set to CH0.
    - Initial delay: The time between the write access and the first edge generation of PWM signal and determined by the value of CM0, CN0 and the clock frequency of the channel
  - Configurable or manually defined initial delay to delay startup of the PWM generator

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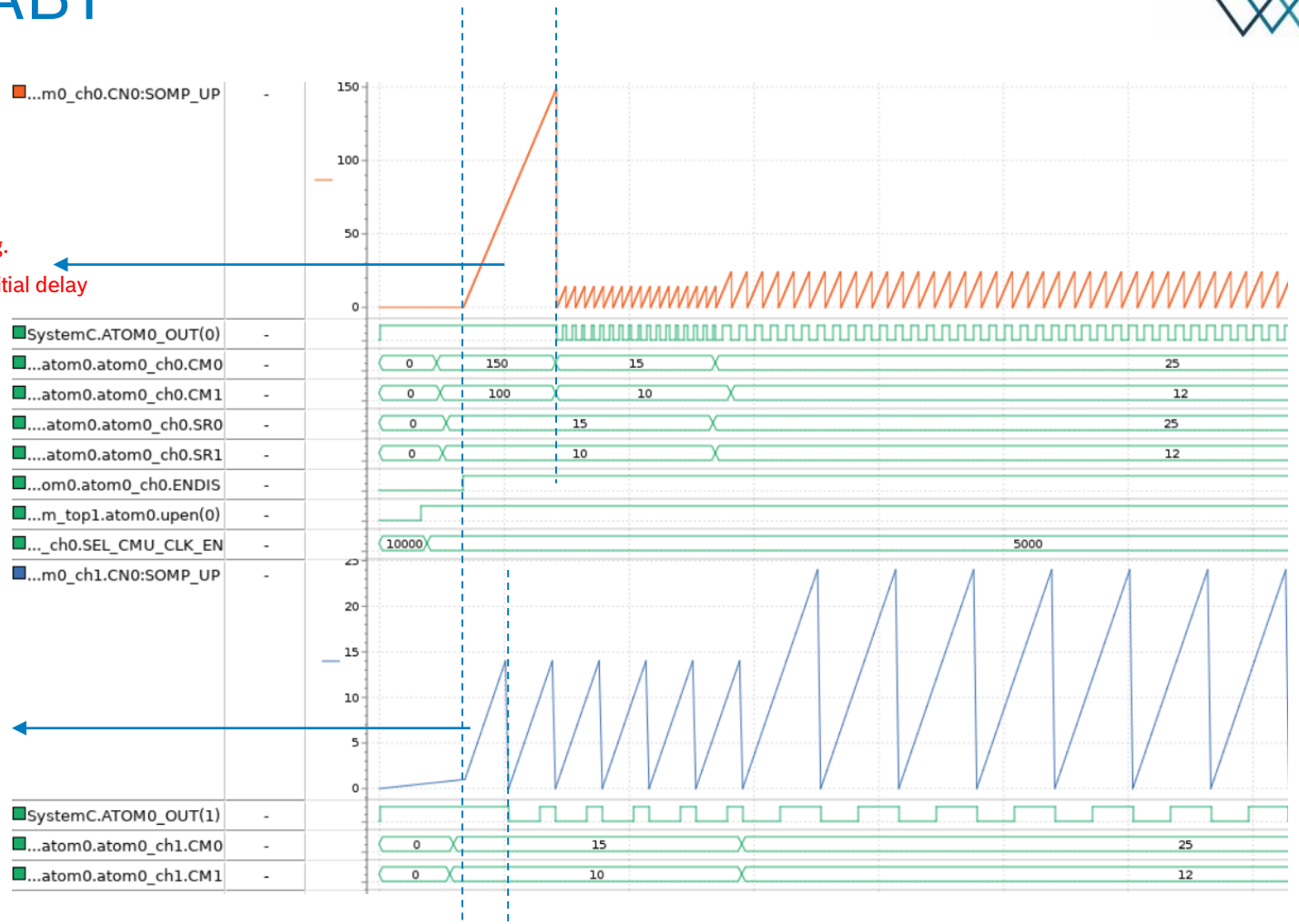
Coside Testcase: ATOM SOMP
Waveforms – LAB1



After enabling channels, the counter starts counting.

But the output is delayed due to the configurated initial delay

Default initial delay

ATOM_CH0

with configurated initial delay

ATOM_CH1

without configurated initial delay

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