

Automotive Electronics

M_CAN IP Module



BOSCH
Invented for life

```
process (BOSCH M_CAN IP)
begin
  if (CAN IP Module in VHDL)
  then

    -- M_CAN

  endif;
end process;
```

M_CAN IP Module

Features

- ▶ Conform with CAN Protocol 2.0 A, B and ISO 11898-1
- ▶ **NEW** CAN FD with max. 8 data bytes supported
- ▶ CAN Error Logging
- ▶ AUTOSAR optimized
- ▶ SAE J1939 optimized
- ▶ Improved acceptance filtering
- ▶ **NEW** Up to 64 dedicated Receive Buffers configurable
- ▶ Two configurable Receive FIFOs
- ▶ Up to 32 dedicated Transmit Buffers configurable
- ▶ Configurable Transmit FIFO
- ▶ Configurable Transmit Queue
- ▶ Configurable Transmit Event FIFO
- ▶ Direct Message RAM access for Host CPU
- ▶ Parity / ECC check for Message RAM (optional)
- ▶ Multiple M_CANs may share the same Message RAM
- ▶ Programmable loop-back test mode
- ▶ Maskable module interrupts, 2 interrupt lines
- ▶ 8/16/32-bit Generic CPU Interface, connectable to customer-specific Host CPUs
- ▶ Two clock domains (CAN clock and Host clock)
- ▶ Power-down support

General description

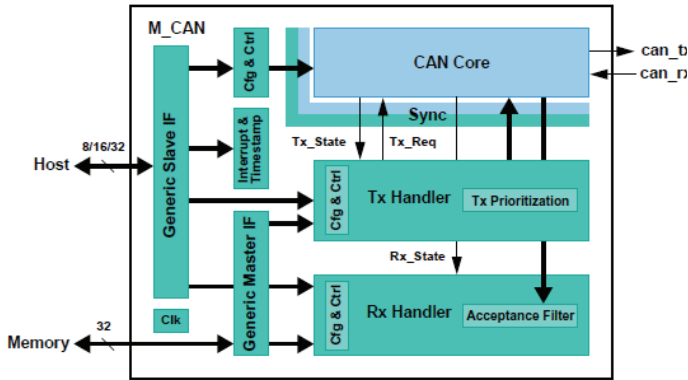
The M_CAN is a CAN IP module that can be realized as a stand-alone device, as part of an ASIC, or as an FPGA. It performs communication according to the Bosch CAN protocol specification 2.0 part A, B and according to ISO 11898-1. It also supports the new CAN FD (CAN with Flexible Data-rate) feature. Additional transceiver hardware is required for connection to the physical layer.

The message storage is intended to be a single- or dual-ported Message RAM outside of the module. It is connected to the M_CAN via the Generic Master Interface. Depending on the chosen integration, multiple M_CAN controllers can share the same Message RAM.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM and provides receive message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core and provides transmit status information.

Acceptance filtering is implemented by a combination of up to 128 filter elements whereas each one can be configured as a range, as a bit mask, or as a dedicated ID filter.

The M_CAN module is delivered with a 32-bit CPU interface. For Altera FPGAs the Altera Avalon bus interface is provided, for Lattice the Wishbone interface. They can easily be replaced by a user-defined module interface.



Block functions and size

CAN_Core

The CAN_Core performs communication according to the CAN protocol version 2.0 A, B and ISO 11898-1. CAN FD is also supported.

Sync

Synchronizes signals between the two clock domains.

Cfg & Ctrl

CAN Core related configuration and control bits.

Interrupt & Timestamp

Interrupt control and 16-bit CAN bit time counter for receive and transmit timestamp generation. An externally generated 16-bit vector may substitute the integrated counter.

Generic Slave Interface

Connects the M_CAN to a wide range of customer CPUs.

Generic Master Interface

Connects the M_CAN access to an external 32-bit Message RAM. A single M_CAN can use at most 1.2k • 32 bit.

Tx Handler

Controls the message transfer from the external Message RAM to the CAN Core. A maximum of 32 Tx Buffers can be configured for transmission. A Tx Event FIFO stores Tx timestamps together with the respective Message ID.

Rx Handler

Controls the transfer of received messages from the CAN Core to the external Message RAM. The Rx Handler supports two Receive FIFOs for storage of up to 64 messages each, and up to 64 dedicated Receive Buffers. An Rx timestamp is stored together with each message. Up to 128 filter elements can be configured for 11-bit IDs and up to 64 for 29-bit IDs.

Approximate size of M_CAN IP module for ASIC design

M_CAN	30.7k gates
Message RAM	max. 38kbits / M_CAN instance

Approximate size of M_CAN IP module for Altera FPGAs

4500 comb. ALUTs + 2200 dedicated regs + 9 M4Ks RAMs*
 *) additional logic for connection to Host CPU and for Message RAM arbitration required

Deliverables for ASIC design

- ▶ Well documented VHDL source code
- ▶ VHDL test bench environment
- ▶ M_CAN User's Manual (programmer's view)
- ▶ M_CAN System Integration Guide (designer's view)
- ▶ M_CAN Module Integration Guide (designer's view)
- ▶ M_CAN Conformance Test Report

Deliverables for FPGA design

- ▶ Altera encrypted VHDL source code or Lattice synthesized core netlist
- ▶ VHDL source code of an example system design with RAM and an example arbiter instance
- ▶ Source code of Altera Avalon bus interface for Altera or Wishbone interface for Lattice
- ▶ M_CAN User's Manual (programmer's view)
- ▶ M_CAN System Integration (designer's view)
- ▶ M_CAN FPGA Integration Guide (designer's view)
- ▶ M_CAN Conformance Test Report
- ▶ Programming examples for fast start up

Supported FPGA families

- ▶ Altera Cyclone, Arria, and Stratix series
- ▶ Lattice ECP and XP series

Regional sales contacts

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