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Resource-efficient MCS programming

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Introduction

- Emulation of communication interfaces using GTM
 - Additional communication interfaces on general purpose I/Os
 - MCS for protocol handling to keep the workload of the main CPU low
 - Multiple communication channels handled by single MCS channel



Single Edge Nibble Transmission



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Features

- 6 data nibbles
- 4-bit CRC calculated over the data nibbles
- Nominal clock period (tick) / unit times (UT) from 3 to 90 μs
- Maximum clock variation +- 20 %
- Successive calibration pulse deviation < 1.5625 % (1/64)
 - 2 different options to handle deviation errors
- Additional serial message channel (slow channel)
 - 1 or bits encoded in 16 consecutive messages
 - Short serial message: 16 bit payload
 - Enhanced serial message: 21 bit payload
 - 6-bit CRC

Signal reception

• TIM channel in PWM measurement mode

Timing constraints:

- Min UT: 3 µs

 20 % clock variation
 Min UT 2.4 µs

 Calibration pulse is 56
 UT long and may vary by 1/64 $\frac{56}{64} * 2.4 us = 2.1 us$
- -> TIM clock higher than 1 MHz should be sufficient
- -> <u>But</u> there is another timing contraint

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Accuracy

• UT = 3 μs, TIM Clk = 25 MHz

Synchronization pulse: $56 \cdot 3 \mu s \cdot 25 \text{ MHz} = 4200 \text{ ticks (TIM)}$ with -20% tolerance = 3360 ticks (TIM)
1UT in TIM ticks: $\frac{3360}{56} = 60$ Worst case: $\frac{3415}{56} = 60.98$ (will be floored to 60)
calc error $\frac{1}{61} = 1.64 \%$

- Multiplies with bits
 - max 15-bit -> last bit will be detected 24.59 % in advance



Unit Time Calculation

• Calculation of $\frac{1}{56}$ using shift and add (backward compatibility to GTM 1.5)

Required precision
 Stay within the registers' word range
 1
 1
 1
 1

$$\bullet \frac{1}{56} = \frac{1}{2^6} + \frac{1}{2^9} + \frac{1}{2^{12}} + \frac{1}{2^{15}} + \frac{1}{2^{18}} + \frac{1}{2^{18}}$$

UT = 90 μs, TIM Clk = 25 MHz

Synchronization pulse: 56 · 90 μs · 25 MHz = 126000 ticks (TIM)

- with +20% tolerance = 151200 ticks (TIM)
- Max. left shift of 6 to stay within 24-bit range of register

$$= \frac{1}{56} = \frac{1}{2^6} + \frac{1}{2^9} + \frac{1}{2^{12}} + \frac{1}{2^{15}} + \frac{1}{2^{18}} + \dots = \left[2^6 + 2^3 + 1 + \frac{1}{2^3} + \frac{1}{2^6} + \dots\right] \frac{1}{2^{12}}$$



System Architecture





Features

- Each SENT channel has [2]:
 - Polling message (periodic messages OS tasks)
 - Interrupt message (sensor synchronous immediately needed by application after reception)

Polling messages will be stored in MCS RAM and transferred by DMA
 DMA is triggered by MCS in configurable time period (e.g. 1ms)

- GTM-FIFO will be used for interrupt message
 - FIFO interrupt after reaching configured watermark



Message Handling

Interrupt message	(24bits)) – GTM-FIFO
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RX Data (6 nibbles) – 24bits CRC – Nibble [23:20] / reserved [19:16] / Valid frame counter

[15:8] / Error flags [7:0]

Timestamp – 24bits

one ARU transfer 2x24bit

one ARU transfer 2x24bit optional – dependent on configuration bit

Polling message	(24bits)) – MCS	RAM
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RX Data (6 nibbles) – 24bits

reserved [19:16] / Valid frame counter [15:8] / Error flags [7:0]

[2]



Conclusion

- I MCS channel can handle up to 4 SENT receivers in parallel (80 MHz sysclk)
- ARU polling is the limiting factor (GTM 1.5 compatible)
 - Bus Master Interface of newer GTM versions allows even more SENT channels per MCS channel
- But since 4 TIM channels can be used by 1 MCS channel
 Available TIM channels and available I/Os are the limiting factor



References

[1] SAE International: SENT—Single Edge Nibble Transmission for Automotive Applications; J2716; Jan 2010

[2] Eugen Becker: 590_360_SW-SENT_Interface; v15; March 3rd, 2016

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