

Accelerating GTM Software Development and Test In the Software and Hardware Supply Chain, by using Virtual Hardware ECUs.

Bart Vanthournout 23/09/2022

Agenda

- Industry Challenges
- Virtual Prototyping
- Supply Chain Enablement with GTM
- GTM reference Model Integration and Features

Five Biggest Automotive Industry Challenges



Supply Chain Disruption

- · Worldwide chip shortage compressing the supply chain
- OEMs, Tier 1s, New Entrants are designing own SoCs

Overhaul of E/E Architectures

- Demand for new HAD/ADAS features, electrified powertrain, infotainment
- New zonal architectures

Complex Software Development & Deployment

- Millions lines of code
- · Software updates over the air
- SW Ecosystems

Increasing Security Challenges

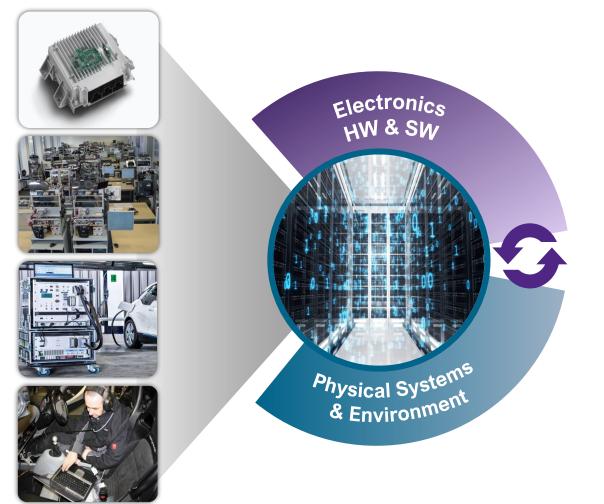
- New vulnerabilities from OTA software updates, self-driving cars, 5G connectivity
- Additional focus on security + safety

Accelerating Time-to-Market to Compete

New automotive entrants challenging traditional processes

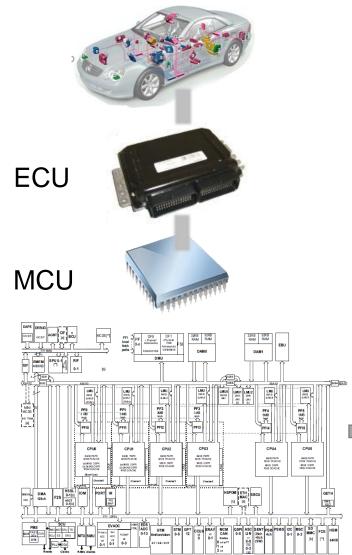
Conquer the Challenges of HW/SW System Validation

Virtual Prototyping Enables a Software-First Mindset

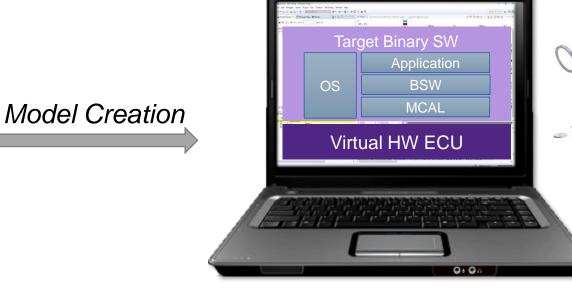


- Supply chain collaboration with executable specification
- ✓ Early SW bring-up
- \checkmark More productive system testing with
 - Software-in-the-Loop
 - Virtual Hardware-in-the-Loop
 - Virtual vehicle
- Supports agile development, continuous integration and delivery
- ✓ Functional safety and security system validation

What is a Virtualizer Development Kit (VDK)?

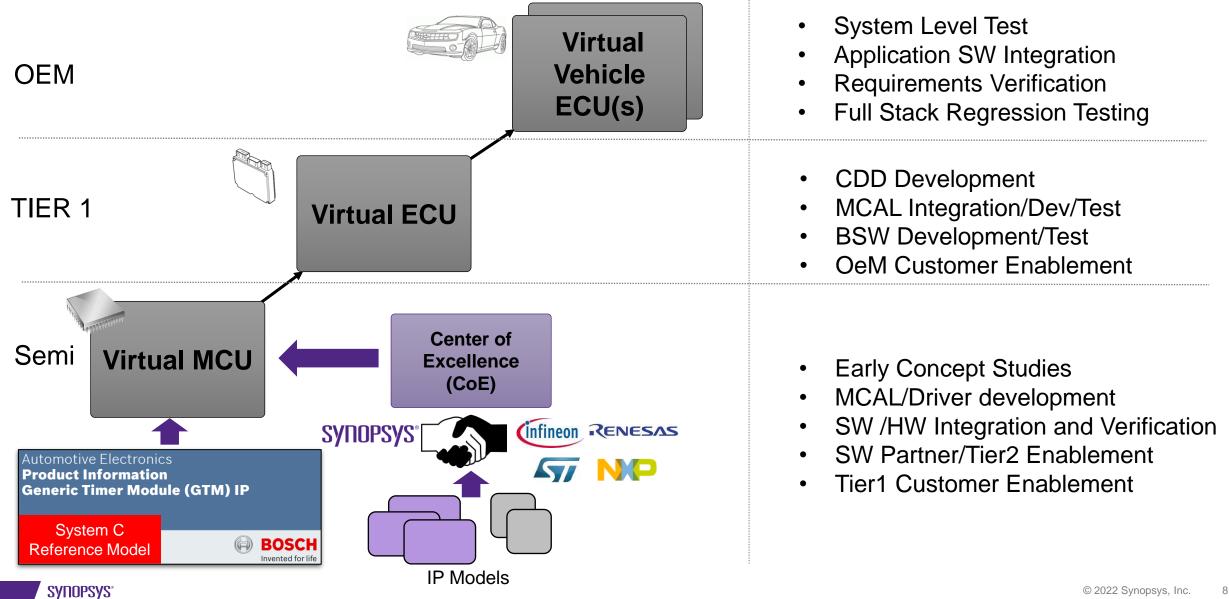


- Fast software model of the digital hardware ECU or MCU
 - Abstracted for Software Execution
- For the purpose of executing unmodified binary production software
 - Without dependency on real hardware
- And providing a higher debugging/analysis efficiency
 - And solving hardware accessibility issues, pre and post silicon



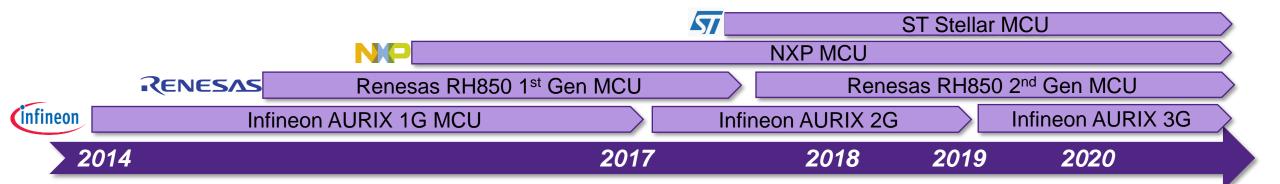


Supply Chain Enablement with GTM use cases



Enabling VDKs with the GTM & Reference Model.

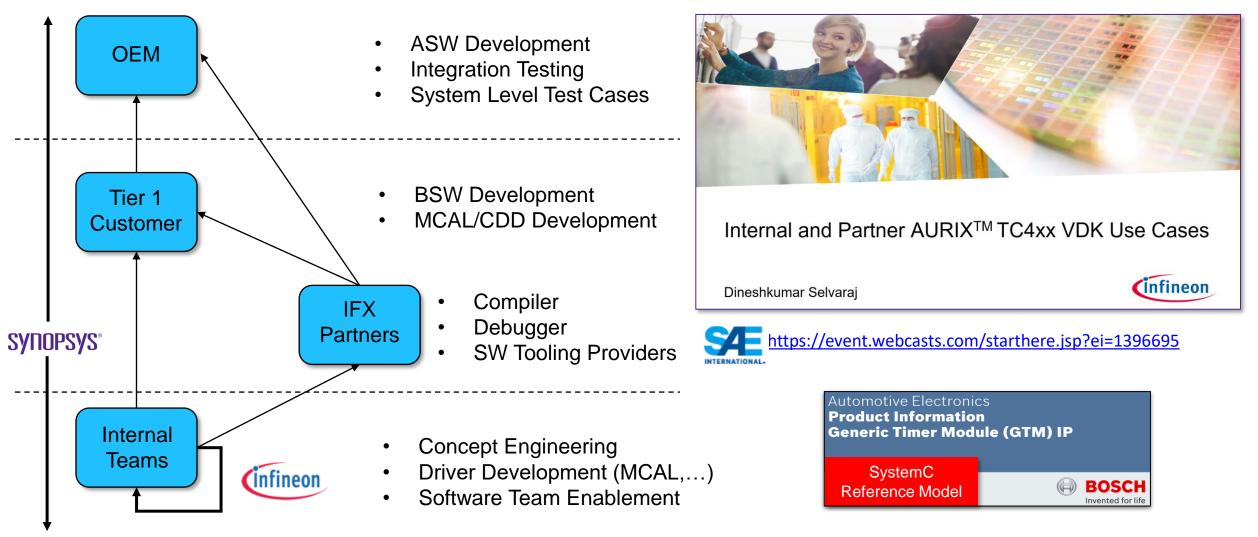
- Multiple VDKs Support GTM Enablement with Multiple Semis
 - SNPS partners with top Semis in Automotive
- Synopsys Integrates Bosch GTM Reference Model Sources.
 - Including enhancements for debugging/analysis and performance
- Synopsys has a long-term relationship with Bosch
 - Delivers feedback from heavy Tier1/OEM usage
 - Delivers feedback and performance enhancements



Semi Customer and Partner Enablement Example

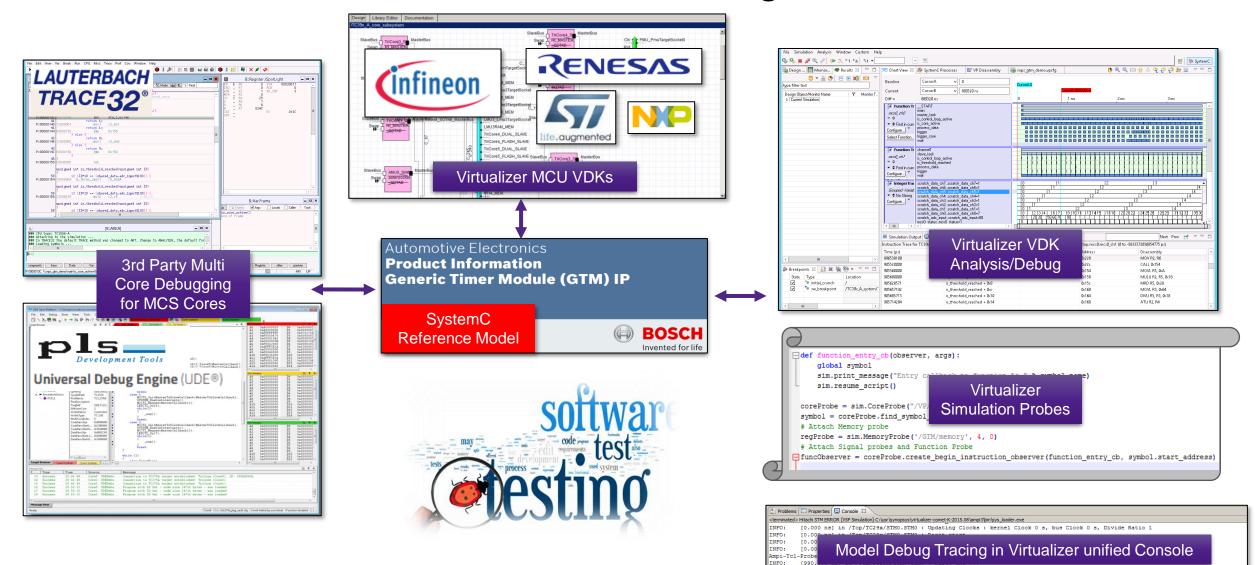






GTM Reference Model Integration Features Enabling development, integration and test in the Supply Chain

Virtualizer GTM Reference Model Integration



INFO:

TNEO.

[990.000 ns]

/TC29x/STM0.STM0 : Fower on Reset is DeAsserted

[990.000 ns] in /Top/TC29x/STM0.STM0 : Clock signal value: 20 ns

Third Party Debugger Tooling - Multicore Capable

| File Edit View Var Break Run CPU Misc Trac | | a=v a | An : # FR Y | 6 1 15 | |
|--|--|---------|--------------------------|------------------------------|---|
| _ | | | e | | СН |
| Note ↓ Diverge ✓ Return ↓ Diverge ✓ Return ↓ L t addr/line code label immemonic t P:00000134 45010020 15_core:retd r r p:00000134 5501020 15_core:retd r r p:00000134 16 (shared_data.statu r p r p:0000138 F500003 atul r p:00000138 F550148 jbs s s r p:0000141 ibs s p:0000144 ibs s p:000144 ibs s p:000144 ibs s p:0000144 ibs s p:0000144 ibs s p:000144 ibs s p:0017 r p:0017 p:017 p:017 p:018 p:017 p:018 p:018 p:018 p:018 | 3:DataList Jp ▶ Go II Break ⊠Mode Go t. → Find comment s I= MCS_MASTER_CHAINEL) { 5.0x3 5.0x3 2.0x1 x150 2.0x0 x150 | | IT NI | | CH |
| <pre>P:00000154 S00000A is_thres.:mov] r unsigned int is_threshold_rea {</pre> | <pre>data.adc_input\$100)) (5.0x64 ched(unsigned int ID) data.adc_input\$100)) (2.r5 ched(unsigned int ID) data.adc_input\$100)) (</pre> | > .if | | ::Var.Frame ✔Ayge ☐Locels | v → 3 Coler Task: = |
| ### Loading symbols < | | × > | < | | ✓ |
| components trace Data Var Li P-0000013C \\arps_gtm_demo\main\is_core_active+0x8 | it PERF SYStem Step Go | Break s | Ymbol Frame 0 stopped | Register other | MIX UP .:: |
| | 13 Success 20 45:48. Core0 1 14 Success 20 46:48. Core2:1 | - | oment Tools bug Engi | •0). 1D 201 ne (UDE® | - 410 0x0000000 D10 A11 0x00000000 D11 A12 0x0000000 D12 C = |

- Support for Full Register Set (PER file)
- MCS memory visibility and interactivity.
- Support for synchronized multicore debugging for MCS channels
 - Synchronised to MCU cores to maximize visibility and correlation.
 - Co-debugging with MCU cores supported
- MCS-asm debugging support
- High Level Language (C/C++) debugging support for MCS engines.

Virtualizer GTM Synchronized Debugging and Visibility

0000

00000

0001

0x00000000

0x00000000

0x00000000

0x00000000

Attach Signal probes and Function Prob

funcObserver = coreProbe.create_begin_instruction_observer(function_entry_cb, symbol.start_address

| - ile Simulation Analysis Window Custom Help | | | | | | | | | | |
|--|---|---|--------------------------|------------------|--|--------------|-----------------------------------|-----------------------------|---------------------|-----------|
| 🗞 🔍 🔳 🖋 🔍 🧭 🕪 🗈 🕛 t 🍡 🖡 👻 | ▼ 22 | | | | | | | | 8 | 🔅 SystemC |
| 🏩 Design Browser 🙁 🔲 Memory Map 🛷 Results | | 5 | • Q ~ | 🞢 Cha | rt View | 🔛 VP Disas | sembly 🖾 🍕 | snps_gtm_dem | » 1 | - 6 |
| /TC39x_A_system/TC39x/Peripheral_System/GTM/i_qtm2 | | tm_top/mcs0/mc | s0_ch0 | | | _ | | | 👌 🚺 = 🏣 = , | 🖗 🗂 🥆 |
| ⊿ # GTM ^ | ltem | Offset | Value | Addr | ess: (0x00 | 0000118) | V 0 | Core: mcs(|) ch0 | |
| ⊿ 🏮 gtm_wrapper | — R0 | | 0x00000000 | | | , | | | | |
| ⊿ 🏮 gtm_top | — R1 | | 0x00000000 | BP | Symbol | A | ddress | Instruction | Disassembly | ^ |
| ⊿ 🌐 mcs0 | — R2 | | 0x0000001 | | <channel7< td=""><td>7+0x8> [</td><td>00000104]</td><td>0xe0030210</td><td>CALL 0x210</td><td></td></channel7<> | 7+0x8> [| 00000104] | 0xe0030210 | CALL 0x210 | |
| 🔯 mcs0_ch0 | — R3 | | 0x00000000 | | <channel7< td=""><td>7+0xc> [</td><td>00000108]</td><td>0xa2800000</td><td>MOV R2, STA</td><td></td></channel7<> | 7+0xc> [| 00000108] | 0xa2800000 | MOV R2, STA | |
| 🕋 mcs0_ch1 | — R4 | | 0x00000022 | | <channel7< td=""><td>7+0×10> [</td><td>0000010c]</td><td>0x42fffffe</td><td>ANDL R2, 0xFFFFFE</td><td></td></channel7<> | 7+0×10> [| 0000010c] | 0x42fffffe | ANDL R2, 0xFFFFFE | |
| ch2 | — R5 | | 0x00000001 | | <channel7< td=""><td>7+0×14> r</td><td>00000110]</td><td>0xa8200000</td><td>MOV STA, R2</td><td></td></channel7<> | 7+0×14> r | 00000110] | 0xa8200000 | MOV STA, R2 | |
| Multi-MCS ^{ch3} | — R6 | | x0000008 | | <is_contro< td=""><td></td><td>00000114]</td><td>0xa5010020</td><td>MRD R5, 0x20</td><td></td></is_contro<> | | 00000114] | 0xa5010020 | MRD R5, 0x20 | |
| ch4 | - R7 Multi-MO | CS Core | x000002ac | _ | <is_contro< td=""><td>l loon</td><td></td><td></td><td>DS O.S</td><td></td></is_contro<> | l loon | | | DS O.S | |
| Channel 📫 🚽 | - CTRI | | x00030011 | - | <is_contro< td=""><td></td><td>Disasse</td><td>mbly Vie</td><td>EW A, 0x5, 0x128</td><td></td></is_contro<> | | Disasse | mbly Vie | EW A, 0x5, 0x128 | |
| Debugging ch6 ch7 | – ACB Registe | er View | x00000000 | | - | Carlo o Plan | | | MOVE R2, 0x1 | |
| | — PC | | .x00000118 | | <is_contro< td=""><td></td><td>00000120]</td><td>0x12000001</td><td>,</td><td>_</td></is_contro<> | | 00000120] | 0x12000001 | , | _ |
| | — МНВ | | 0x00000000 | | <is_contro< td=""><td></td><td>00000124]</td><td>0xe0000130</td><td>JMP 0x130</td><td></td></is_contro<> | | 00000124] | 0xe0000130 | JMP 0x130 | |
| 🝘 mcs1 ch0 | - CTRG | | 0x00000000 | | <is_contro< td=""><td></td><td>00000128]</td><td>0x12000000</td><td>MOVL R2, 0x0</td><td></td></is_contro<> | | 00000128] | 0x12000000 | MOVL R2, 0x0 | |
| 🖉 mcs1_ch1 | - STRG | | 0x00000000 | | <is_contro< td=""><td></td><td>0000012c]</td><td>0xe0000130</td><td>JMP 0x130</td><td></td></is_contro<> | | 0000012c] | 0xe0000130 | JMP 0x130 | |
| mcs1_ch2 | - ERR | | 0x00000000 | | <is_contro< td=""><td>ol_loop [</td><td>00000130]</td><td>0xe0040000</td><td>RET</td><td></td></is_contro<> | ol_loop [| 00000130] | 0xe0040000 | RET | |
| @ mcs1_ch3 | - CTRL STAT | | 0x00000000 | | <is_core_a< td=""><td>active + 0 [</td><td>00000134]</td><td>0xa5010020</td><td>MRD R5, 0x20</td><td></td></is_core_a<> | active + 0 [| 00000134] | 0xa5010020 | MRD R5, 0x20 | |
| mcs1_ch4 | - RESET | | 0x00000000 | | <is_core_a< td=""><td>active+0 [</td><td>00000138]</td><td>0x75000003</td><td>ATUL R5, 0x3</td><td></td></is_core_a<> | active+0 [| 00000138] | 0x75000003 | ATUL R5, 0x3 | |
| mest ch5 | - CAT | | 0x00000000 | | <is_core_a< td=""><td>active + 0 [</td><td>0000013c]</td><td>0xe8510148</td><td>JBS STA, 0x5, 0x148</td><td></td></is_core_a<> | active + 0 [| 0000013c] | 0xe8510148 | JBS STA, 0x5, 0x148 | |
| 🍘 mcs1_ch6 🗸 | - CWT | | 0x00000000 | | <is a<="" core="" td=""><td>active + 0</td><td>000001401</td><td>0x12000001</td><td>MOVL R2. 0x1</td><td></td></is> | active + 0 | 000001401 | 0x12000001 | MOVL R2. 0x1 | |
| < III > | | | | | | | | 0:00:0 | 0.003 582 800 000 | |
| | | | | | | | | I | | |
| etails 🚺 Memory 🔀 | 👲 📑 🛃 🗤 | | | - Q ∖ | ~ | | | | | |
| irtual @ /TC39x_A_system/TC39x/Core_System/TriCore0 : 0x0 <vp explorer="" td="" tra<=""><td>aditional> 🛛 🕂 New Renderings</td><td>M_REGS/m_regs/AT(</td><td>OM6_CH2_RDADDR Offset</td><td></td><td>alue 🛆</td><td>A</td><td></td><td></td><td></td><td></td></vp> | aditional> 🛛 🕂 New Renderings | M_REGS/m_regs/AT(| OM6_CH2_RDADDR Offset | | alue 🛆 | A | | | | |
| Goto Address: 0x00000000100011 | | ATOM5_AGC_AC | | 0x0000 | | | | | | |
| | | ATOM5_AGC_OU | - | 0x0000 | | ⊟def f | unction_entry_cb(obser | ver, args): | | |
| 25 03 03 10 00 00 00 01 00 00 00 00 00 00 00 00 | | ATOM5_AGC_OU ATOM5_AGC_FUF | | 0x0000 | | | lobal symbol | | | |
| 0x0000000F0100010 00 00 00 00 00 00 00 00 00 00 00 | | ATOM5_AGC_FOR ATOM5_AGC_INT | | 0x0000 0x0000 | | - | <pre>im.print_message("Entr</pre> | y callback to function %s " | symbol.name) | _ |
| | | | - | | Dlfe | | <u>\ /:</u> t. | | 1 | |
| 0x0000000F0100020 00 00 00 00 19 11 0F 00 00 00 00 00 04 00 | - 00 00 · · · · · · · · · · · · · · · · | | | e | JILE | | | Ializor_S | Imiliation_ | |
| | - | - G1 | TM Confia | o | 0000 | a | VIRU | | imulation | |
| 0x00000000666100020 00 00 00 00 19 11 0F 00 00 00 00 00 04 00 0x0000000610100 0x000000061100 Memory Views | | G | TM Config Register | 0 0 | | 01 8] | VIRU | Jalizer S Script | | |

Interactivity

ATOM5_CH1_IRQ_NOTIFY_0xf8a0

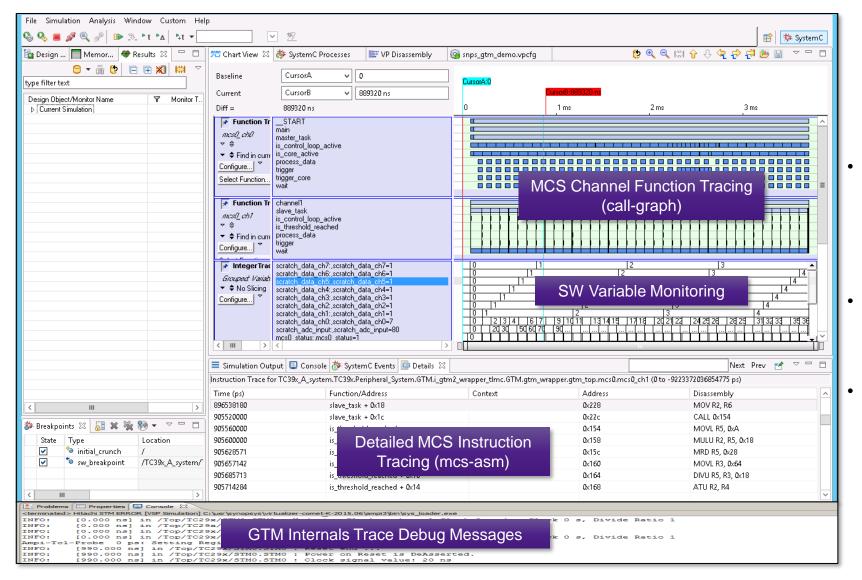
ATOM5_CH1_IRQ_EN
 0xf8a4

- ATOM5_CH1_IRQ_FORCIN_0xf8a8

- ATOM5_CH1_IRQ_MODE 0xf8ac

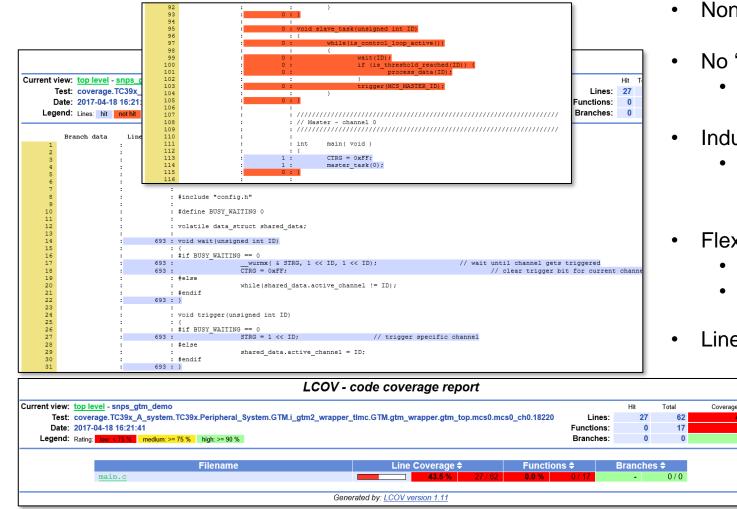
- All MCS executable Channels instrumented as Virtualizer "Cores".
- Seamless Channel switching with MCU cores and GTM MCS "cores"
- Interactive MCS Register Views
- Interactive Config Register Views
- Virtualizer Debugger Scripting supported for integrated system debugging.

Virtualizer GTM Tracing and Analysis



- Virtualizer Integration for Software Analysis
 - MCS Function Call-Graph Tracing
 - MCS Instruction Tracing
 - GTM config register tracing
 - MCS Memory access tracing
- Integrated GTM Ref Model "Internals" tracing in unified console.
 - · Controlled via scripting or interactively
- Viewing and Debugging in context of mainline MCU SW execution.

Virtualizer GTM MCS Code Coverage Solution.



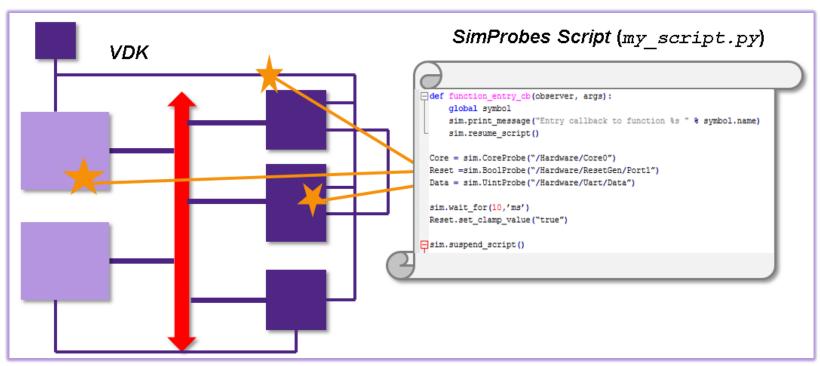
- Non-Intrusive Code Coverage for high level language MCS.
- No 'gcov' code modifications needed in MCS code
 - Uses Virtualizer's non-intrusive instrumentation
- Industry standard LCOV Reports.
 - Intermediate formats available for custom report generation
- Flexible MCS channel coverage reports
 - Can be per MCS channel or
 - Single merged multi MCS channel report
- Line, Branch and Function coverage stats

16

Virtualizer Simulation Probes

(stimulus, fault injection, and analysis)

- GTM integration is compatible with Virtualizer Simulation Probes
- What is Virtualizer Simulation Probes.
 - An in-simulation python scripting framework for fault injection, signal stimulus and analysis.



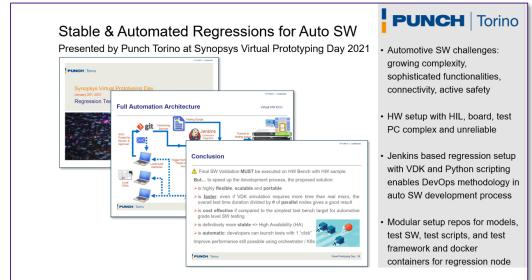
- Allows you to override and control signals anywhere in the MCU VDK model
- Override and control mechanisms are uniquely supported in the Synopsys SystemC kernel.
- Unlimited number of scripts allowed to run in parallel.
- It runs inside simulation process , so has high simulation speed.

Practical GTM use Case on Powertrain Virtual HIL (vHIL)

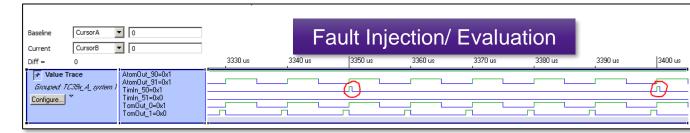
• Target –

•

- Reliable testing methodology with regressions
- Replacing HIL stimulus with scripted stimulus
 - Crank/Cam/Injection....
- Methodology -
 - Scriptable waveform generation for repeatable stimulus scenarios.
 - Inject faults into input stimulus or output signals to establish system impact.
 - Custom analysis for debugging purpose
 - Regression environment (CI/CD, Jenkins...)
 - VDK including an integrated GTM reference model critical part of the verification.

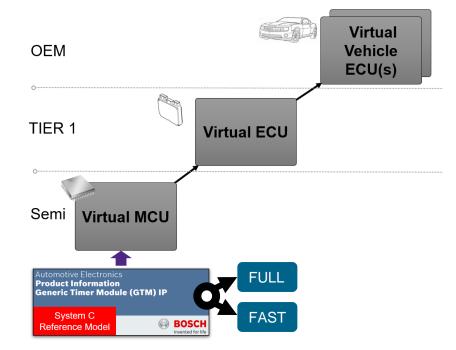


| Baseline CursorA 💌 | 0 | CursorA:0 | |
|---------------------------|--|-----------------|---------------------|
| Current CursorB Diff = 0 | 0 | CursorB () O | Stimulus Generation |
| Grouped: TC39k_A_system i | AtomDut_90=0x1 AtomDut_91=0x1 TimIn_50=0x1 TimIn_51=0x0 TomDut_0=0x1 TomDut_1=0x0 | | |



Working with GTM through the supply chain

- There is a need for more abstractions as we move up the design chain and systems become more complex
 - Mixing different representations VDK, Silver, ...
- GTM is used along the supply chain from Semi to OEM
 - We need an "Optimized Fast GTM" based on the use case
 - OEMs can often get away with some abstraction of detail
 - Tier1 and Semi may not need all details, especially if GTM is not the focus of a particular test
- Use a switchable GTM model
 - A combination of the reference model with a more abstract implementation
 - User can decide which one to use, full detail or fast model





- Virtual Prototypes are essential to address today's automotive design challenges
- The GTM is a critical component of many MCUs and requires advanced debugging and analysis features to fully exploit its feature set
- Synopsys has a comprehensive solution around the GTM enabling SW development in the context of the full system at any point along the supply chain
- Synopsys is actively involved in integrating and optimizing the GTM reference model provided by BOSCH.



Thank You